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(71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL)**

(72) Inventors; and

(75) Inventors/Applicants (for US only): **VAN DER WOLF, Pieter [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). VAN EIJDHOVEN, Josephus, T., J. [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven**

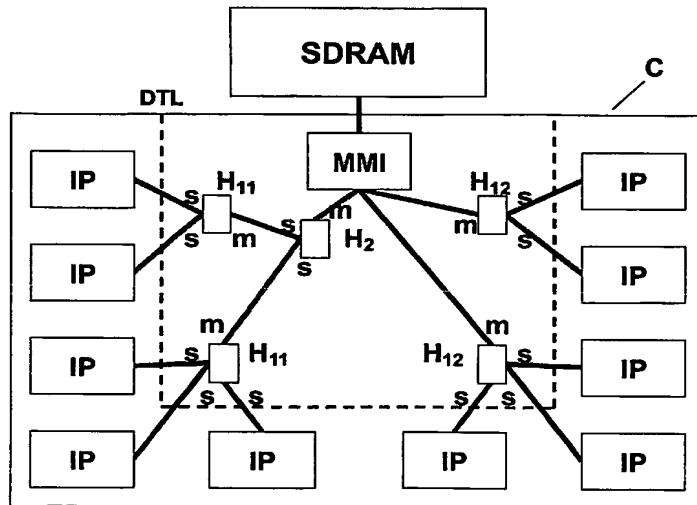
(74) Agent: **DE JONG, Durk, J.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL)**

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(54) Title: DATA PROCESSING SYSTEM



(57) Abstract: The disclosed data processing system comprises a memory means (SDRAM), a plurality of data processing means (IP) provided for accessing to said memory means (SDRAM), and a communication interface means coupled between said memory means (SDRAM) and said plurality of data processing means (IP), said communication interface means including a network of nodes (H 11, H 12, H2), each node comprising at least one slave port (s) for receiving a memory access request from a data processing means (IP) or from a previous node and at least one master port (m) for issuing a memory access request to a next node or to said memory means (SDRAM) in accordance with the memory access request received at said slave port (s), wherein said at least one slave port (s) is connected to a master port (m) of a previous node or to one of said data processing means (IP) and said at least one master port (m) is connected to a slave port (s) of a next node or to said memory means (SDRAM).

**Declaration under Rule 4.17:**

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